

Random Dopant-Induced Fluctuations of Electrical Characteristics in Nanoscale Single- and Double-Gate MOSFETs

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Abstract—In this paper, we explore random dopant-induced fluctuations of electrical characteristics for sub-65 nm metal-oxide-semiconductor field effect transistors (MOSFETs). Numerical calculation of fluctuations is performed by solving a quantum correction model with perturbation and monotone iterative methods. Accuracy of simulation is firstly verified with the measured data from fabricated 65 nm planar MOSFETs. Fluctuations of the threshold voltage and the drain current are compared between single- and double-gate (SG and DG) MOSFETs. Compared with the results of the SG MOSFET, it is found that the DG MOSFET has the smaller fluctuations with respect to different device channel length, device width, and channel doping. The suppression of fluctuations is mainly due to nature of device's gate structure and good channel controllability. This numerical technique is computationally cost-effective and can be incorporated into technology computer-aided design (TCAD) tool for device simulation.

Keywords—Electrical characteristics, fluctuation, random dopant, perturbation technique, modeling, simulation, TCAD, nanodevices, single- and double-gate MOSFETs

I. INTRODUCTION

Multiple gate nanoscale metal-oxide-semiconductor field effect transistors (MOSFETs) have recently been of great interests [1], [2]. Random nature of ion implantation and diffusion processes results in significantly random fluctuations in these nanodevices [3]–[5]. They affect the design window, yield, noise margin, stability, and reliability of ultra large-scale integration (ULSI) circuits. Monte Carlo simulation and small signal analysis of transport equations have been proposed to explore the fluctuation-related issues in semiconductor devices [6], [8], [9]. Unfortunately, these methods are either computationally expensive or not suitable for industrial TCAD applications. Recently, the fluctuation of threshold voltage for bulk MOSFET has been explored by considering a quantum correction model [7] which is solved with a perturbation technique [3]. The corresponding nonlinear system is solved with the monotone iterative method [10]. We believe that studying the fluctuation of electrical characteristics for the nanoscale single- and double-gate (SG and DG) MOSFETs will benefit device fabrication and ULSI circuit design in sub 65-nm technology era.

In this paper, the fluctuation of the threshold voltage and drain current of the SG and DG MOSFETs are computed and compared by solving an extended quantum correction model. The quantum correction of electron density is performed in a set of drift-diffusion equations. To account the random dopant-induced fluctuations, the whole set of equations is solved with the perturbation and monotone iterative methods. Accuracy of simulation is

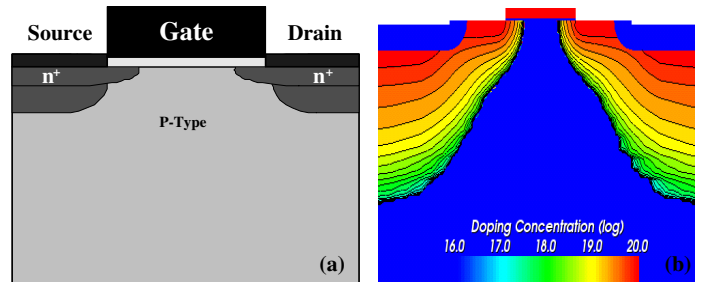


Fig. 1. (a) The device structure and (b) the doping profile of the investigated 65nm bulk N-MOSFET

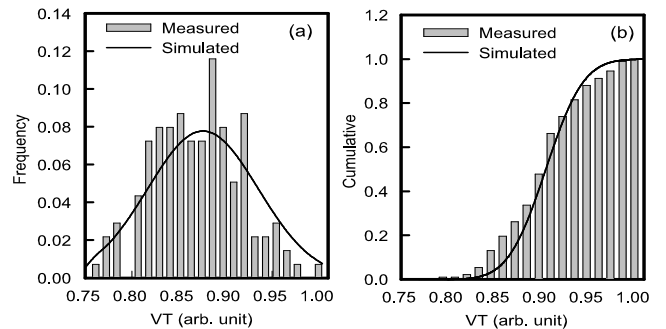


Fig. 2. (a) The distribution and (b) cumulative distribution of the threshold voltage for the investigated 65 nm N-MOSFET, where bar is the measurement and solid line is the simulated result.

successfully verified with the measured data from the fabricated 65 nm planar polysilicon gate MOSFET. Fluctuations of the threshold voltage and the on-state current are explored between SG and DG MOSFETs. The DG MOSFET has the smaller fluctuations due to the nature of device's gate structure and good channel controllability. This paper is organized as follows. Sec. II shows the computational model for the random dopant-induced fluctuations. Sec. III presents the results and discussion. Finally, we draw the conclusions.

II. THE SIMULATION METHODOLOGY

For the investigated SG and DG MOSFETs, shown in Fig. 3, a set of two-dimensional (2D) drift-diffusion equation together with quantum correction to electron density is numerically solved for the quantum corrected electrostatic potential. With the computed quantum corrected potential and electron density distribution over entire device structure, we consider the following perturbations to the original equations

$$D(x_i, y_j) = \hat{D}(x_i, y_j) + \tilde{D}(x_i, y_j), \quad (1)$$

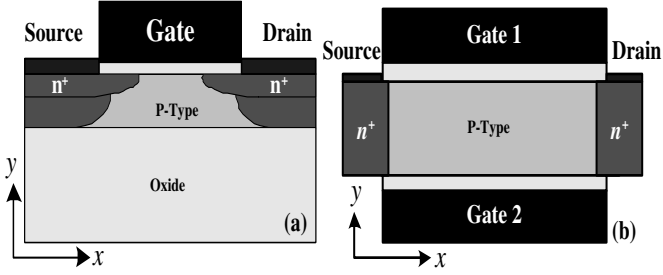


Fig. 3. Cross-section views of the (a) SG and (b) DG MOSFETs.

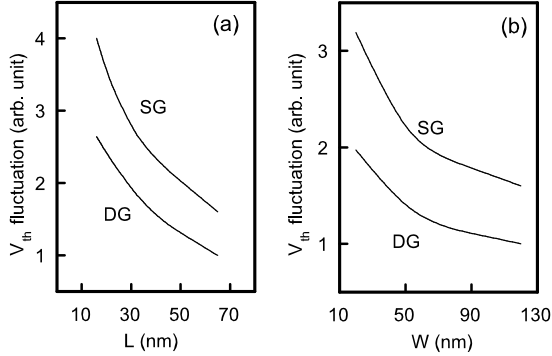


Fig. 4. Plot of the standard deviation of the threshold voltage versus (a) the channel length and (b) the device width for the simulated SG and DG MOSFETs, where $T_{ox} = 1.5$ nm and $N_A = 5e17$ cm $^{-3}$.

$$\phi_{QM}(x_i, y_j) = \hat{\phi}_{QM}(x_i, y_j) + \tilde{\phi}_{QM}(x_i, y_j), \quad (2)$$

$$n_{QM} = \hat{n}_{QM} + \tilde{n}_{QM}, p = \hat{p} + \tilde{p}, \quad (3)$$

where D is the doping profile, " $\hat{\cdot}$ " means that the expected value of D , ϕ , n and p , and " $\tilde{\cdot}$ " is their fluctuation, respectively. In Eqs. (1)-(3), ϕ_{QM} and n_{QM} are the quantum corrected potential and electron density; p is the hole density. The positions (x_i, y_j) for all i and j are the discretized mesh points. We compute the fluctuation of threshold voltage and drain current with the randomly perturbed quantum potential, electron and hole density. Thus, the fluctuations σ_{vth} and σ_{id} are computed by assuming that the doping concentration are independent random variables at each mesh point (x_i, y_j) for all i and j .

III. RESULTS AND DISCUSSION

For the 65 nm planar polysilicon gate bulk N-MOSFET, shown in Fig. 1a, a calibrated doping profile, shown in Fig. 1b, is adopted and simulated to calculate the corresponding threshold voltage fluctuation. With the computed σ_{vth} and assuming a normal distribution, we plot the distribution of the threshold voltage, shown in Fig. 2. The simulated threshold voltage is 0.383 V and the corresponding standard deviation σ_{vth} is 0.028 V. There are about one hundred samples are measured and used in this investigation. Our simulation shows a good agreement with the measurement, and then confirms the accuracy of this approach.

As shown in Fig. 3, we explore the σ_{vth} versus the channel length L and device width W for the SG SOI and DG devices. It is found that σ_{vth} decreases nonlinearly (σ_{vth} is inversely proportional to square root of $L \times W$) when L and W increases for the two devices, shown

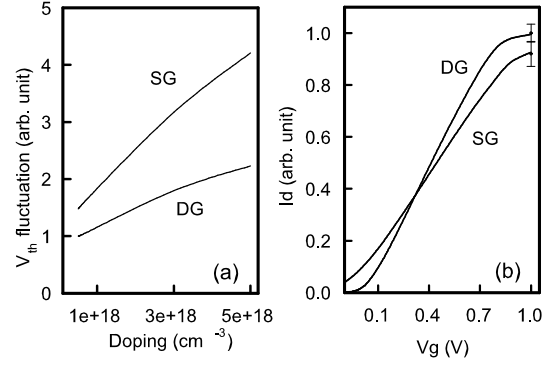


Fig. 5. (a) Plot of σ_{vth} versus the doping level for the simulated SG and DG MOSFETs, where $L = 65$ nm, $W = 50$ nm and $T_{ox} = 1.5$ nm. (b) Plot of the I_d - V_d curves for the simulated SG and DG MOSFETs, where $L = 25$ nm, $W = 10$ nm, $T_{ox} = 1.0$ nm, $N_A = 1e17$ cm $^{-3}$ and $V_d = 1.0$ V. The bar indicates its fluctuation.

in Fig. 4. Figure 5a shows the standard deviation σ_{vth} versus the doping level. As shown in Fig. 5a, both structures predict that the σ_{vth} increases when the constant doping level increases. The result of DG MOSFET shows the more stable and smaller fluctuation of the threshold voltage. With this computational model, we preliminarily calculate the on-state current fluctuation for the 25 nm SG and DG MOSFETs with the same doping level, shown in Fig. 5b. The drain current fluctuation σ_{id} of the DG device is about 4.5% for the corresponding drain current and is about 6.5% for the SG SOI device. The smaller σ_{id} appearing in DG device is due to the better channel controllability. We note that device structure will play a crucial role in reduction of fluctuations of electrical characteristics in sub-45 nm technology node and beyond.

IV. CONCLUSIONS

The random dopant-induced fluctuations of the threshold voltage and the on-state current have been studied for sub-65 nm SG and DG MOSFETs. To calculate the variance of the physical quantities, a set of quantum corrected drift-diffusion equations have been solved with perturbation technique. Compared with measured data of 65 nm N-MOSFET, this approach has shown good accuracy. Compared with SG MOSFET, DG device potentially shows the smaller fluctuations.

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