Element-based Topological Index Reduction for Differential-Algebraic Equations in Circuit Simulation

Simone Bächle, Falk Ebert

***Abstract*— In this paper we will discuss certain aspects of the transient simulation of electrical circuits. It is a well known problem that DAEs in circuit simulation may possess a higher index (e.g. 2) and thus exhibit undesirable numerical behaviour. While methods for the reduction of the higher index exist, they are usually algebraic in nature. The large size of the systems in VLSI circuit simulation prohibits the use of algebraic methods for index reduction. We will present a topological approach to index reduction that changes certain elements of the circuit netlist to obtain a circuit DAE with usually greatly improved numerical behaviour.**

I. Introduction

SIMULATION of electrical circuits is a commonly used tool to test new electrical circuits prior to producing an actual prototype. Especially in chip design it is important to be able to have a quick and reliable method for simulating the behaviour of a circuit. But, in this context, the respective circuits tend to contain millions of elements, thus, making simulation difficult, just because of the sheer size of the problem.

The main methods for the simulation of circuits are the Modified Nodal Analysis (MNA), the charge-/flux-oriented MNA (MNA c/f) and the Sparse Tableau Approach (STA), cf. [1]. Kirchhoff's Laws and branch constitutive relations (BCR) are set up to form a system of equations describing the important properties of the circuit, e.g., voltages and currents.

As this system contains differential relations as well as algebraic ones, it is called 'Differential-Algebraic-Equation' (DAE). A well known problem of DAEs is that besides obvious algebraic relations, they may contain so-called hidden constraints that are revealed only by differentiating certain equations or parts thereof. In circuit simulation, these DAEs are known to have index 2, given some topological properties of the network. This higher index leads to several undesirable effects in the numerical solution of the DAEs. Recent approaches try to lower the index of DAEs to improve the numerical behaviour. These methods usually involve costly algebraic transformations of the equations. Especially, for large scale circuit equations, these transformations become too costly to be efficient.

Institut für Mathematik, MA 3-3, Technische Universität Berlin, Straße des 17. Juni 136, D-10623 Berlin, Germany, {baechle, ebert}@math.tu-berlin.de.

Supported by MATHEON, the DFG Research Center "Mathematics for key technologies".

The hidden constraints in the case of the MNA and the MNA c/f have been determined, see [2], and in [3] it has been shown, how they can be obtained without algebraic transformations of the circuit equations by only using information contained in the topology of the circuit. The information obtained in this way has until now mainly been used to determine consistent initial values, fulfilling the hidden constraints as well, for numerical integration of the circuit equations. Recently, a concept called *minimal extension*, see [4], has been used to include the hidden constraints into the process of integration, see [5]. The DAE obtained in this way is of index 1, while, especially large scale systems, can be of index 2. DAEs of higher index than 1 are usually unstable with respect to numerical integration, i.e., they are usually more costly to solve, while accuracy might suffer as well.

We will take a different approach to the topological analysis, one that focuses on index reduction. It will be shown that it is possible to incorporate the hidden constraints into the network equations while retaining the MNA or MNA c/f structure of the equations. The method proposed here will use the results of the topological index analysis on a circuit element level. The main advantage will be, that no algebraic transformations of the circuit equations will have to be performed, but the method will change the circuit itself. Hence, prior to the actual simulation, a preprocessing step will have to be performed, analyzing the structure of the circuit and exchanging certain elements by newly defined elements, in order to obtain a circuit that possesses a DAE of index 1. The virtue of this approach is that after the preprocessing, no more algebraic transformations have to be performed, but the netlist, i.e., the list containing all structure- and element related information, itself is changed. The changed netlist can then be processed by the same simulation tools as the original netlist, provided they are able to handle the introduced new elements. As the new netlist produces circuit equations of index 1, the integration process is usually much faster and more accurate than for the index 2 case. The linear systems arising from discretization are better conditioned. Additionally, it is much easier to obtain a set of consistent initial values for the index 1 case. The only extra cost is a one-time preprocessing step, while existing software can be used for integration of the equations. A tool called *ETICS* (**E**lement-based **T**opological **I**ndex reduction in **C**ircuit **S**imulation) that performs this preprocessing step is in preparation.

II. Element replacement

The main topological properties of a circuit that are responsible for a higher-index behaviour are CV loops, i.e., loops formed by branches that are occupied by capacitances or voltage sources, and LI cutsets, i.e., cutsets formed by branches containing inductances and current sources only. For every loop and every cutset, an orientation can be chosen. A more detailed description of these structures is given in [6]. Here, only CV loops will be considered. Loops of voltage sources and cutsets of current sources are generally not allowed, because they might produce meaningless equations.
We will derive expressions for the hidden constraints in such a way that the steps needed to perform an index reduction become clearly visible. Consider one specific CV loop. Let n_C^{loop} and $n_V^l oop$ be the number of capacitances and voltage sources in the loop, respectively. The hidden constraint arising from that CV loop can be interpreted as follows:

- Denote the voltages across capacitances in the loop by $v_{C,j}^{loop},\ j = 1 \dots n_C^{loop}$ the loop),
- denote the voltages across $v_{s,j}^{loop},\ j = 1 \dots n_V^{loop}$ (number of voltage sources in the loop).
- Set $\alpha_{*,j} = \pm 1$, where $* \in \{C, V\}$. For every element in the loop, the constant $\alpha_{*,j}$ is 1 if the element is oriented in the same way as the loop and -1 otherwise.
- Kirchhoff's voltage law over that loop states that

$$\sum_{j=1}^{n_C^{loop}} \alpha_{C,j} v_{C,j}^{loop} + \sum_{j=1}^{n_V^{loop}} \alpha_{V,j} v_{s,j}^{loop} = 0. \qquad (1)$$

- The derivative of (1) holds as well,

$$\sum_{j=1}^{n_C^{loop}} \alpha_{C,j} \frac{d}{dt} v_{C,j}^{loop} + \sum_{j=1}^{n_V^{loop}} \alpha_{V,j} \frac{d}{dt} v_{s,j}^{loop} = 0. \qquad (2)$$

As the currents through capacitances depend on the derivatives of the respective capacitance voltages, equation (2) imposes a constraint on the branch currents as well. This constraint is not originally visible in the system and has been obtained by differentiation, thus representing a hidden constraint.
We want condition (2) to be fulfilled, hence, it has to appear explicitly in the circiut equations. For this purpose, we choose one of the involved capacitances. Without loss of generality, we assume that this is C_1^{loop} and that the direction of the loop is identical to the one of the capacitance. The corresponding voltage is $v_{C,1}^{loop}$. Then, we split (2) as follows

$$\frac{d}{dt} v_{C,1}^{loop} = - \sum_{2}^{n_C^{loop}} \alpha_{C,j} \frac{d}{dt} v_{C,j}^{loop} - \sum_{1}^{n_V^{loop}} \alpha_{V,j} \frac{d}{dt} v_{s,j}^{loop}. \qquad (3)$$

We multiply this equation by C_1^{loop} to obtain

$$\begin{aligned} i_{C,1} = C_1^{loop} \frac{d}{dt} v_{C,1}^{loop} \quad = \quad & - \sum_{2}^{n_C^{loop}} \alpha_{C,j} C_1^{loop} \frac{d}{dt} v_{C,j}^{loop} \\ & - \sum_{1}^{n_V^{loop}} \alpha_{V,j} C_1^{loop} \frac{d}{dt} v_{s,j}^{loop}. \qquad (4) \end{aligned}$$

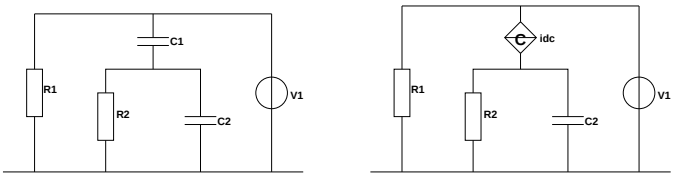

Fig. 1. Test circuit of index 2 (left) and circuit after element replacement (right)

	orginal System	with DCS	emulated DCS
system size	3	3	5
function evaluations	2363	397	187
time steps	432	73	34
accuracy	1E-4	2E-7	2E-7

TABLE I
TEST RESULTS WITH RADAU5 AND TOL = 1E-8

By definition, the term $C_1^{loop} v_{C,1}^{loop}$ describes the charge q_1^{loop} of the capacitance and $C_1^{loop} \frac{d}{dt} v_{C,1}^{loop} = \frac{d}{dt} q_1^{loop}$ is the current through this capacitance. In this way, we have expressed one branch current explicitly. Hence, we can remove the capacitance C_1^{loop} and replace it by a current source that provides the current given by the right hand side of (4). This differentially controlled current source (DCS) may again be interpreted as a current controlled current source when the controlling derivatives of capacitance voltages are taken as currents through these capacitances (emulated DCS). This, however, will usually lead to the introduction of additional elements to measure the current through the capacitances. These re-interpretations of the capacitance C_1^{loop} do not change the analytical solution of the circuit equations. The numerical properties of the circuit, however, have changed in such a way that constraint (2) now explicitly appears among the equations and will thus be respected by the numerical method used to solve the equations.
A similar approach can be taken for LI cutsets, cf. [6].

III. Numerical Tests

We consider the small linear test circuit in Fig. 1. The element replacement procedure has been applied to this circuit an the capacitance C_1 has been replaced by a differentially controlled current source. Some test results with the DCS and an emulated DCS are shown in Table I.

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